6502 Instruction Set

HI	LO-NIBBLE															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
00	BRK impl	ORA X,ind	??? ---	??? ---	??? ---	ORA zpg	ASL zpg	??? ---	PHP impl	ORA #	ASL A	??? ---	??? ---	ORA abs	ASL abs	??? ---
10	BPL rel	ORA ind,Y	??? ---	??? ---	??? ---	ORA zpg,X	ASL zpg,X	??? ---	CLC impl	ORA abs,Y	??? ---	??? ---	??? ---	ORA abs,X	ASL abs,X	??? ---
20	JSR abs	AND X,ind	??? ---	??? ---	BIT zpg	AND zpg	ROL zpg	??? ---	PLP impl	AND #	ROL A	??? ---	BIT abs	AND abs	ROL abs	??? ---
30	BMI rel	AND ind,Y	??? ---	??? ---	??? ---	AND zpg,X	ROL zpg,X	??? ---	SEC impl	AND abs,Y	??? ---	??? ---	??? ---	AND abs,X	ROL abs,X	??? ---
40	RTI impl	EOR X,ind	??? ---	??? ---	??? ---	EOR zpg	LSR zpg	??? ---	PHA impl	EOR #	LSR A	??? ---	JMP abs	EOR abs	LSR abs	??? ---
50	BVC rel	EOR ind,Y	??? ---	??? ---	??? ---	EOR zpg,X	LSR zpg,X	??? ---	CLI impl	EOR abs,Y	??? ---	??? ---	??? ---	EOR abs,X	LSR abs,X	??? ---
60	RTS impl	ADC X,ind	??? ---	??? ---	??? ---	ADC zpg	ROR zpg	??? ---	PLA impl	ADC #	ROR A	??? ---	JMP ind	ADC abs	ROR abs	??? ---
70	BVS rel	ADC ind,Y	??? ---	??? ---	??? ---	ADC zpg,X	ROR zpg,X	??? ---	SEI impl	ADC abs,Y	??? ---	??? ---	??? ---	ADC abs,X	ROR abs,X	??? ---
80	??? ---	STA X,ind	??? ---	??? ---	STY zpg	STA zpg	STX zpg	??? ---	DEY impl	??? ---	TXA impl	??? ---	STY abs	STA abs	STX abs	??? ---
90	BCC rel	STA ind,Y	??? ---	??? ---	STY zpg,X	STA zpg,X	STX zpg,Y	??? ---	TYA impl	STA abs,Y	TXS impl	??? ---	??? ---	STA abs,X	??? ---	??? ---
A0	LDY #	LDA X,ind	LDX #	??? ---	LDY zpg	LDA zpg	LDX zpg	??? ---	TAY impl	LDA #	TAX impl	??? ---	LDY abs	LDA abs	LDX abs	??? ---
B0	BCS rel	LDA ind,Y	??? ---	??? ---	LDY zpg,X	LDA zpg,X	LDX zpg,Y	??? ---	CLV impl	LDA abs,Y	TSX impl	??? ---	LDY abs,X	LDA abs,X	LDX abs,Y	??? ---
C0	CPY #	CMP X,ind	??? ---	??? ---	CPY zpg	CMP zpg	DEC zpg	??? ---	INY impl	CMP #	DEX impl	??? ---	CPY abs	CMP abs	DEC abs	??? ---
D0	BNE rel	CMP ind,Y	??? ---	??? ---	??? ---	CMP zpg,X	DEC zpg,X	??? ---	CLD impl	CMP abs,Y	??? ---	??? ---	??? ---	CMP abs,X	DEC abs,X	??? ---
E0	CPX #	SBC X,ind	??? ---	??? ---	CPX zpg	SBC zpg	INC zpg	??? ---	INX impl	SBC #	NOP impl	??? ---	CPX abs	SBC abs	INC abs	??? ---
F0	BEQ rel	SBC ind,Y	??? ---	??? ---	??? ---	SBC zpg,X	INC zpg,X	??? ---	SED impl	SBC abs,Y	??? ---	??? ---	??? ---	SBC abs,X	INC abs,X	??? ---

Address Modes:

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A      .... Accumulator         OPC A          operand is AC
abs    .... absolute            OPC $HHLL      operand is address $HHLL
abs,X  .... absolute, X-indexed OPC $HHLL,X    operand is address incremented by X with carry
abs,Y  .... absolute, Y-indexed OPC $HHLL,Y    operand is address incremented by Y with carry
#      .... immediate           OPC #$BB       operand is byte (BB)
impl   .... implied             OPC            operand implied
ind    .... indirect            OPC ($HHLL)    operand is effective address; effective address is value of address
X,ind  .... X-indexed, indirect OPC ($BB,X)    operand is effective zeropage address; effective address is byte (BB) incremented by X without carry
ind,Y  .... indirect, Y-indexed OPC ($LL),Y    operand is effective address incremented by Y with carry; effective address is word at zeropage address
rel    .... relative            OPC $BB        branch target is PC + offset (BB), bit 7 signifies negative offset
zpg    .... zeropage            OPC $LL        operand is of address; address hibyte = zero ($00xx)
zpg,X  .... zeropage, X-indexed OPC $LL,X      operand is address incremented by X; address hibyte = zero ($00xx); no page transition
zpg,Y  .... zeropage, Y-indexed OPC $LL,Y      operand is address incremented by Y; address hibyte = zero ($00xx); no page transition
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