U1
EPM7128SL84
+5V

R1
1k2
C9
10p
GND

C3M58 11 I/O
C3M58 10 I/O
C7M 9 I/O
PRAS 8 I/O
C07X 6 I/O/NC
RW 5 I/O
AN3 4 I/O
Q3 2 OE2/GClk2
1 GClr
C14M 84 OE1
83 GClk1
PCAS 81 I/O
RW80 80 I/O
PHI1 79 I/O/NC
CASEN 77 I/O
EN80 76 I/O
PHI0 75 I/O

VccINT VccINT VccIO VccIO VccIO VccIO VccIO VccIO
3 43 78 66 53 38 26 13

I/O 12 DelayIn/Out[0]
TDI 14
I/O 15
I/O 16 DelayIn/Out[1]
I/O 17
I/O 18 DelayIn/Out[2]
I/O 20
I/O 21 DelayIn/Out[3]
TMS 22
23
I/O 24 RA10
I/O 25 RA11
I/O 27 CAS
I/O 28 RD4
I/O 29 RD5
I/O 30 RD6
I/O 31 RD7

VD3 74 I/O
MD3 73 I/O
TDO 71
VD4 70 I/O
MD4 69 I/O
VD2 67 I/O
MD5 65 I/O
VD5 64 I/O
VD1 63 I/O
TCK 62
MD1 61 I/O
VD6 60 I/O
MD6 58 I/O
VD0 56 I/O
MD7 55 I/O
VD7 54 I/O

I/O 33 RD0
I/O 34 RD1
I/O 35 RD2
I/O 36 RD3
I/O 37 RWE
I/O/NC 39 RAS
I/O 40 RA9
I/O 41 RA8
I/O 44 MA7
I/O 45 MA0
I/O 46 MA1
I/O 48 MA3
I/O 49 MA3
I/O 50 MA4
I/O 51 MA5
I/O/NC 52 MA6

GND GND GND GND GND GND GND GND
7 82 72 59 47 42 32 19
GND

U2
DRAM_2Mx8
+5V

1 VDD
RD0 2 I/O0 A0 10 MA0
RD1 3 I/O1 A1 11 MA2
RD2 4 I/O2 A2 12 MA4
RD3 5 I/O3 A3 13 MA6
RD4 24 I/O4 A4 16 MA5
RD5 25 I/O5 A5 17 MA3
RD6 26 I/O6 A6 18 MA1
RD7 27 I/O7 A7 19 MA7
CAS 23 CAS A8 20 RA8
RAS 7 RAS A9 21 RA9
WE 6 WE A10 9 RA10
OE 22 OE A11/NC 8 RA11
GND 28
GND

J1
ApplelleAux

C3M58 1 60 ENTMG
Vid7M 2 59 C7M
SYNC 3 58 GR
PRAS 4 57 RA10
VC 5 56 RA9
C07X 6 55 FRCTXT
WNDW 7 54 SEGB
SEGA 8 53 Q3
MA7 9 52 RW
MA1 10 51 MA0
ROMEN1 11 50 AN3
ROMEN2 12 49 MA2
MA4 13 48 MA3
MA5 14 47 H0
VD7 15 46 MA6
MD7 16 45 VD0
MD6 17 44 MD0
VD6 18 43 MD1
VD5 19 42 VD1
MD5 20 41 VD2
MD4 21 40 MD2
VD4 22 39 MD3
PHI0 23 38 VD3
CLRGAT 24 37 CASEN
80VID 25 36 PHI1
EN80 26 35 RW80
ALTVID 27 34 LDPS
SEROUT 28 33 PCAS
ENVID 29 32 C14M
+5V 30 31
GND

MD0 MD0
MD1 MD1
MD2 MD2
MD3 MD3
MD4 MD4
MD5 MD5
MD7 MD7

VD0 VD0
VD1 VD1
VD2 VD2
VD3 VD3
VD4 VD4
VD5 VD5
VD6 VD6
VD7 VD7

MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7

H1 H2 H3 H4

FID1 Fiducial   FID2 Fiducial   GND
FID3 Fiducial   FID4 Fiducial

FRCTXT

AN3

+5V
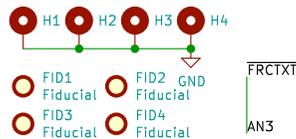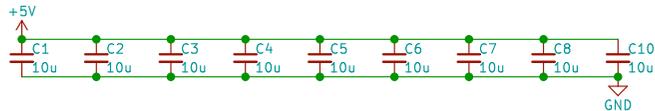C1 C2 C3 C4 C5 C6 C7 C8 C10
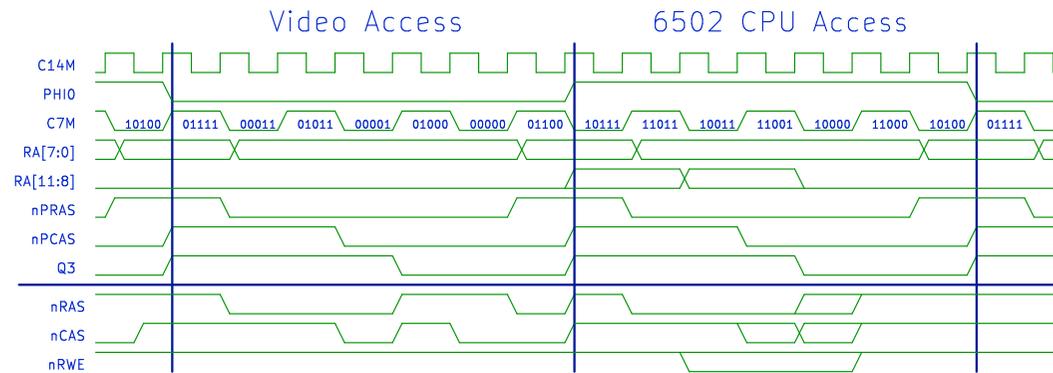10u 10u 10u 10u 10u 10u 10u 10u 10u
GND

Sheet: Docs
File: Docs.sch

Garrett's Workshop
Sheet: /
File: RAM2E.sch
Title: RAM2E
Size: USLetter   Date: 2019-10-13   Rev: 0.9
KiCad E.D.A. kicad (5.1.2-1)-1   Id: 1/2

Video Access   6502 CPU Access

C14M
PHI0
C7M
RA[7:0]   10100 / 01111 / 00011 / 01011 / 00001 / 01000 / 00000 / 01100 / 10111 / 11011 / 10011 / 11001 / 10000 / 11000 / 10100 / 01111
RA[11:8]
nPRAS
nPCAS
Q3

nRAS
nCAS
nRWE

State = { PHI0, C7M, nPRAS, nPCAS, Q3 }

Information may be out of date, superseded by ./cpld/RAM2E.v