

Sheet: Docs
File: Docs.sch

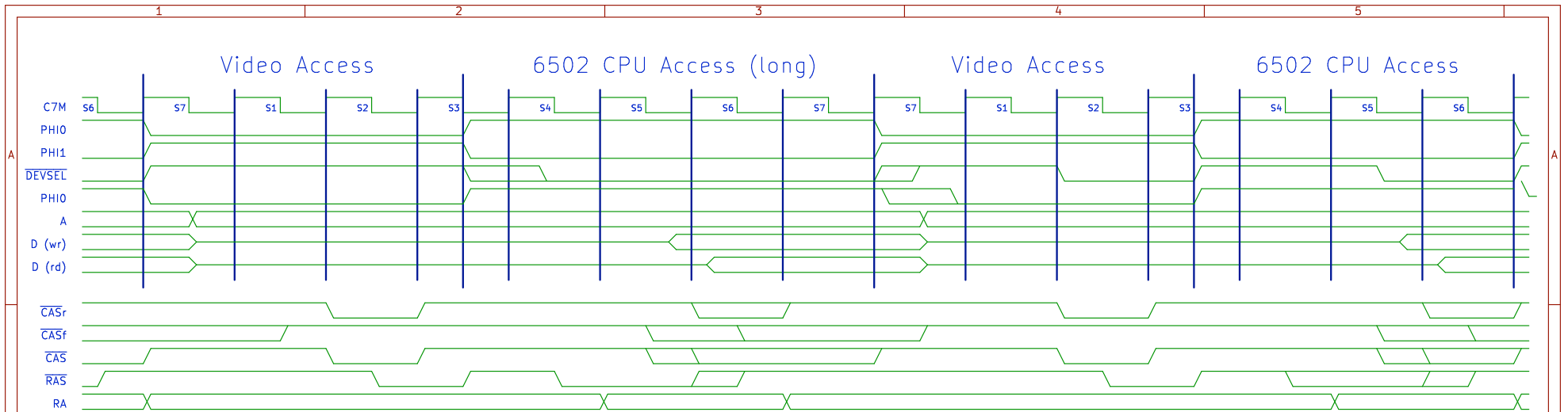
Garrett's Workshop

Sheet: /
File: GR8RAM.sch

Title: GR8RAM

Size: USLetter Date: 2019-10-13
KiCad E.D.A. kicad (5.1.2-1)-1

Rev: 0.9
Id: 1/2



State Synchronization

PHIOreg = PHIO @ C7M
 S[3:0] = (PHIO & PHIOreg) ? 1 : S0 ? 0 : S+1 @ C7M

Select Signals

BankSEL = A==XXF & DEVSEL & REGEN
 RAMSEL = A==XXX3 & DEVSEL & REGEN
 RAMSELreg = S3 ? RAMSEL : RAMSELreg
 AddrHSEL = A==XXX2 & DEVSEL & REGEN
 AddrMSEL = A==XXX1 & DEVSEL & REGEN
 AddrLSEL = A==XXX0 & DEVSEL & REGEN
 REGEN = (IOSEL & S3) ? 1 : REGEN @ C7M
 IOROMEN = (A==XXFF & IOSTRB & S3) ? 0 :
 (A==XX00 & IOSEL & S3) ? 1 :
 IOROMEN @ C7M

Refresh Skip Counter

Ref[3:0] = S1 ? Ref[3:0] : Ref[3:2]==3 ? 0 : Ref[3:0]+1 @ C7M

ROM / DRAM Control

DBEN = S2 & S3 @ C7M
 RCS = IOSEL | (IOSTRB & IOROMEN)
 ROE = RW
 RWE = RW & (DEVSEL | IOSEL | IOSTRB)
 CASr = (S1 & Ref[3:0]==0) | (S5 & RAMSEL) @ C7M
 CASf = ((S5 & RW) | S6 | S7) & RAMSEL @ C7M
 RASf = (S4 & RAMSEL) | (S5 & RAMSEL & RW) | (S2 & Ref[3:0]==0) @ C7M
 CAS0 = CASr | (CASf & DEVSEL & Addr[22])
 CAS1 = CASr | (CASf & DEVSEL & Addr[22])

Address Bus Routing

RA[10:8] = (RAMSEL & (S4 | S5)) ? Addr[10:8] : Addr[21:19] @ C7M
 RA[7:1] = RAMSEL ? (S4 ? Addr[7:1] : Addr[18:12]) : Bank[6:0] @ C7M
 RA[0] = RAMSEL ? (S4 ? Addr[0] : Addr[11]) : A[11] @ C7M

6502-Accessible Registers

Bank[6:0] = (S6 & BankSEL & RW) ? D[6:0] : Bank[6:0] @ C7M
 Addr[22:16] = (S6 & AddrHSEL & RW) ? D[6:0] : Addr[22:16] @ C7M
 Addr[15:8] = (S6 & AddrMSEL & RW) ? D[7:0] : Addr[15:8] @ C7M
 Addr[7:0] = (S6 & AddrLSEL & RW) ? D[7:0] : Addr[7:0] @ C7M
 if (S1 & RAMSELreg) Addr[22:0]++ @ C7M

Data Bus Routing

RD[7:0] = (RW & RES) ? D[7:0] : 8'bZ
 D[7:0] = (DBEN & RW & RES & (DEVSEL | IOSEL | (IOSTRB & ROMEN))) ?
 AddrHSEL ? {1'b1, Addr[22:16]} :
 AddrMSEL ? Addr[15:8] :
 AddrLSEL ? Addr[7:0] :
 RD[7:0] : 8'bZ

Information here may be out of date,
 superseded by ./cpld/GR8RAM.v

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