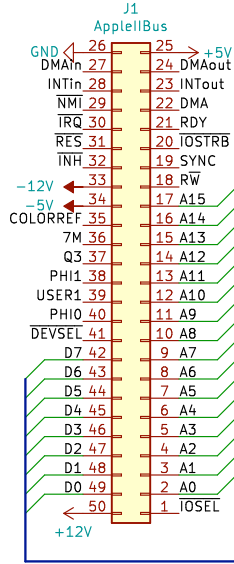
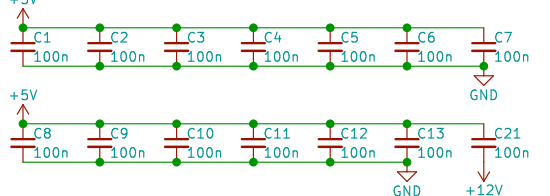
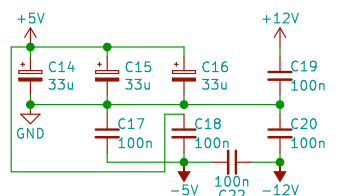
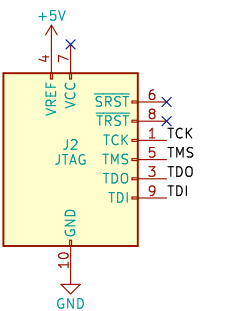
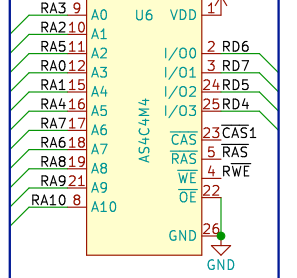
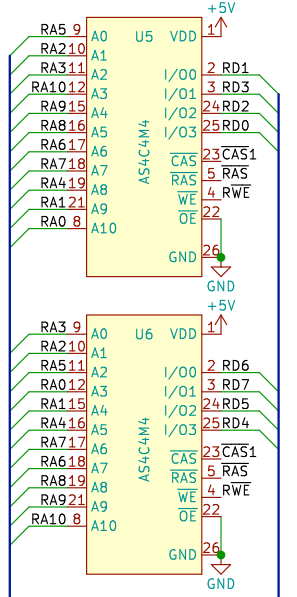
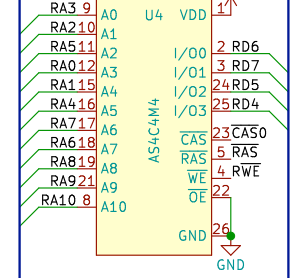
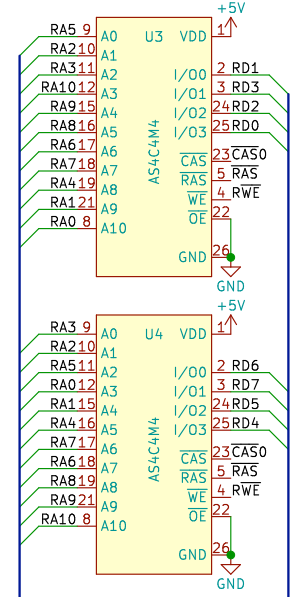
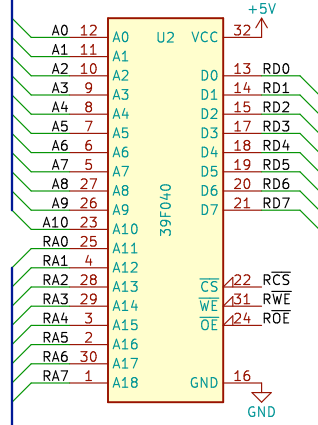
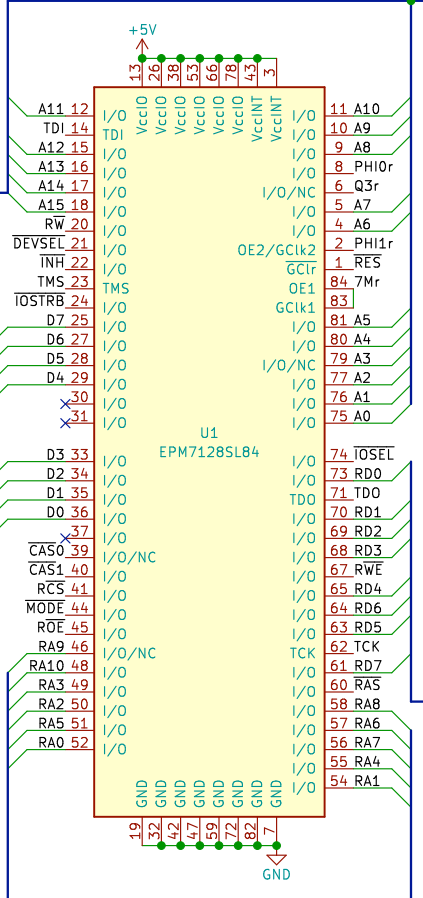
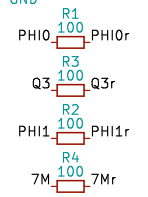
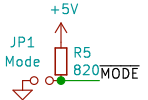
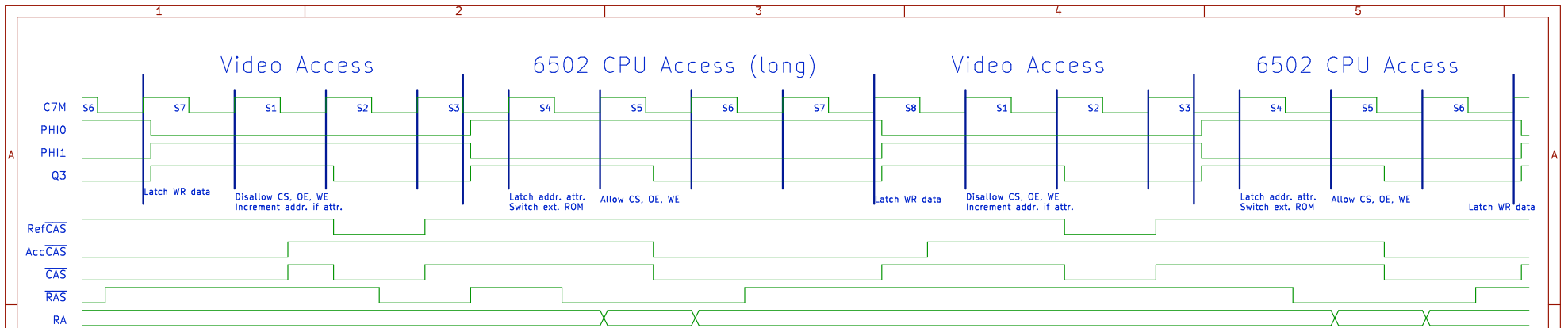


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DMAIn\_DMAOut  
INTIn\_INTOut





### State Synchronization

```
PHI0reg = PHIO @ C7M
S[3:0] = (PHIO & PHI0reg) ? 1 :
        (S==0) ? 0 : S+1 @ C7M
```

### Select signals (registered)

```
BankSEL = S3 ? (A==XXXF & DEVSEL & REGEN) : BankSEL @ C7M
RAMSEL = S3 ? (A==XXX3 & DEVSEL & REGEN) : RAMSEL @ C7M
AddrHSEL = S3 ? (A==XXX2 & DEVSEL & REGEN) : AddrHSEL @ C7M
AddrMSEL = S3 ? (A==XXX1 & DEVSEL & REGEN) : AddrMSEL @ C7M
AddrLSEL = S3 ? (A==XX00 & DEVSEL & REGEN) : AddrLSEL @ C7M
```

```
REGEN = (IOSEL & S3) ? 1 : REGEN @ C7M
IOROMEN = (A==XXFF & IOSTRB & S3) ? 0 :
          (A==XX00 & IOSEL & S3) ? 1 :
          IOROMEN @ C7M
```

### ROM / DRAM Control

```
CSEN = S4 | S5 | S6 | S7 @ C7M
RCS = (IOSEL | (IOSTRB & IOROMEN)) & CSEN
ROE = RW
```

```
RWE = RW & (DEVSEL | IOSEL | IOSTRB)
RAS = (RAMSEL & (S4 | S5)) | S2 @ C7M
RefCAS = S1 @ C7M
AccCAS = RAMSEL & (S5 | S6 | S7) @ C7M
CAS0 = (RefCAS) | (AccCAS & Addr[22] & DEVSEL)
CAS1 = (RefCAS) | (AccCAS & Addr[22] & DEVSEL)
```

### Address Bus Routing

```
RA[10:8] = S4 ? Addr[10:8] : Addr[21:19] @ C7M
RA[7:0] = RAMSEL ? (S4 ? Addr[7:0] : Addr[18:11]) :
         IOSEL ? 8'h00 : Bank[7:0] @ C7M
```

### 6502-Accessible Registers

```
Addr[22:16] = (S6 & AddrHSEL & RW) ? D[6:0] : Addr[22:16] @ C7M
Addr[15:8] = (S6 if AddrMSEL & RW) ? D[7:0] : Addr[15:8] @ C7M
Addr[7:0] = (S6 if AddrLSEL & RW) ? D[7:0] : Addr[7:0] @ C7M
if (RAMSEL & S1) Addr[22:0]++ @ C7M
Bank[7:0] = (S6 & BANKREG & RW) ? D[7:0] : Bank[7:0] @ C7M
```

### Data Bus Routing

```
RD[7:0] = (DEVSEL | RW) ? 8'bZ : D[7:0]
D[7:0] = (CSEN | DEVSEL | RW) ? 8'bZ :
        AddrHSEL ? {1'b1, Addr[22:16]} :
        AddrMSEL ? Addr[15:8] :
        AddrLSEL ? Addr[7:0] :
        RD[7:0]
```

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**Title: GR8RAM**

Size: USLetter Date: 2019-07-23  
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**Rev: 0.1**  
Id: 2/2